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10/678,412	10/02/2003	Jin-Ho Kim	9903-072	9985

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EXAMINER	
VIGUSHIN, JOHN B	

ART UNIT	PAPER NUMBER
2841	

DATE MAILED: 10/19/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

PTO-90C (Rev. 10/03)

Office Action Summary	**Application No.** 10/678,412	**Applicant(s)** KIM, JIN-HO	
	Examiner John B. Vigushin	**Art Unit** 2841	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 October 2003*.
2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.
3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.
4a) Of the above claim(s) _____ is/are withdrawn from consideration.
5)☐ Claim(s) _____ is/are allowed.
6)☒ Claim(s) *1,4-6,8,10-13,18 and 20* is/are rejected.
7)☒ Claim(s) *2,3,7,9,17 and 19* is/are objected to.
8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.
10)☒ The drawing(s) filed on *02 October 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a)☒ All b)☐ Some * c)☐ None of:
1.☒ Certified copies of the priority documents have been received.
2.☐ Certified copies of the priority documents have been received in Application No. _____.
3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *1003/02 Oct 2003*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. Claims 4 and 20 are objected to because of the following informalities:

In Claim 4 contains a typographical error: In line 2, "pads electrically connected to" should be replaced by --pads for electrically connecting--.

In Claim 20, line 5: the second occurrence of "chip" (i.e., after "area") should be deleted.

In Claim 20, line 7: –the-- should be inserted before "chip".

2. Appropriate correction is required.

Rejections Based On Prior Art

3. The following references were relied upon for the rejection hereinbelow:

Behlen et al. (US 5,598,033)	Taniguchi et al. (US 6,388,333 B1)
Asada (US 6,239,496 B1)	Nishimura et al. (US 6,781,241 B2)

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States

> only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims 1, 4-6, 8, 10, 11, 13-16, 18 and 20 are rejected under 35 U.S.C. 102(b) as being anticipated by Taniguchi et al.

As to Claim 1, Taniguchi et al. discloses, in Figs. 19, 20, 21A and 21B (Figs. 21A and 21B being variations of Figs. 19 and 20; col.14: 66-col.15: 1), a plurality of stacked packages including an upper package and a lower package, each package comprising: a board 21 having located on a first side thereof a chip installation area and a bump pad area; at least one chip 3 disposed in the chip installation area; a plurality of redistribution patterns (the wiring patterns that are inclusive of bonding pads 5 and ball pads 8) formed on the board 21 and electrically connected to the chip 3 (Fig. 19 and col.14: 26-32); a plurality of first bump pads 8 formed in the bump pad area which are electrically connected to the redistribution patterns (bond pads 8 labelled in Fig. 19 and not labeled in Figs. 21A,B); a plurality of second bump pads 8 are formed on a second side of board 21 (best seen in Fig. 19); and a plurality of via holes 22 through which the second bump pads 8 are electrically connected to the redistribution patterns (best seen in Fig. 19; col.14: 31-38; the redistribution patterns being inclusive of bonding pads 5 and ball pads 8 as indicated in col.14: 26-31), wherein the respective packages are electrically connected by connecting bump pads 8 of the upper of the two adjacent packages to the first bump pads 8 of the lower package, the chip installation area of the upper and lower packages not being in vertical alignment with each other (Figs. 21A,B and col.15: 4-9).

As to Claim 4, Taniguchi et al. further discloses conductive bumps 7C are provided on the second bump pads 8 for electrically connecting the second bump pads 8 of the upper of two adjacent packages to the first bump pads 8 of the lower package (Figs. 19 and 21A,B).

As to Claim 5, Taniguchi et al. further discloses an encapsulation member 2 surrounding chip 3 for protecting chip 3 from the external environment (Figs. 21A,B; col.14: 29-31; col.15: 1-4).

As to Claim 6, Taniguchi et al. further discloses conductive bumps 7 (i.e., the bumps on the lower package 21) are provided having similar heights to the height of the encapsulation member 2 (Figs. 21A,B; col.14: 54-57).

As to Claim 8, Taniguchi et al. further discloses at least on electronic device 3 (i.e., the device 3 on the second side of the upper package board 21), and is electrically connected to the first bump pads 8 of the upper package (Figs. 19 and 21A,B; best seen in Fig. 19).

As to Claim 10, Taniguchi et al. discloses, in Figs. 19, 20, 21A and 21B (Figs. 21A and 21B being variations of Figs. 19 and 20; col.14: 66-col.15: 1), a plurality of stacked packages including an upper package and a lower package, each package comprising: a board 21 having located on a first side thereof a chip installation area and a bump pad area; at least one chip 3 disposed in the chip installation area; a plurality of redistribution patterns (the wiring patterns that are inclusive of bonding pads 5 and ball pads 8) formed on the board 21 and electrically connected to the chip 3 (Fig. 19 and col.14: 26-32); and a plurality of first bump pads 8 formed in the bump pad area which are electrically connected to the redistribution patterns (bond pads 8 labelled in Fig. 19 and not labeled in Figs. 21A,B), wherein the respective packages are electrically connected by connecting bump pads 8 of the upper package to bump pads 8 of the lower package, the chip installation area of the upper and lower packages not being in vertical alignment with each other (Figs. 21A,B and col.15: 4-9).

As to Claim 11, Taniguchi et al. further discloses an encapsulation member 2 surrounding chip 3 for protecting chip 3 from the external environment (Figs. 21A,B; col.14: 29-31; col.15: 1-4).

As to Claim 13, Taniguchi et al. further discloses conductive bumps 7 (i.e., the bumps on the lower package 21) are provided having similar heights to the height of the encapsulation member 2 (Figs. 21A,B; col.14: 54-57).

As to Claim 14, Taniguchi et al. further discloses at least on electronic device 3 (i.e., the device 3 on the second side of the upper package board 21), and is electrically connected to the first bump pads 8 of the upper package (Figs. 19 and 21A,B; best seen in Fig. 19).

As to Claim 15, Taniguchi et al. further discloses a plurality of second bump pads 8 are formed on a second side of board 21 (best seen in Fig. 19), and a plurality of via holes 22 through which the second bump pads 8 are electrically connected to the redistribution patterns (best seen in Fig. 19; col.14: 31-38; the redistribution patterns being inclusive of bonding pads 5 and ball pads 8 as indicated in col.14: 26-31).

As to Claim 16, Taniguchi et al. further discloses the packages are electrically connected by connecting the second bump pads 8 of the upper of two adjacent packages to the first bump pads 8 of the lower package (by way of bumps 7C; Figs. 19 and 21A,B).

As to Claim 18, Taniguchi et al. further discloses conductive bumps 7C are provided on the second bump pads 8 for electrically connecting the second bump pads 8 of the upper package to the first bump pads 8 of the lower package (Figs. 19 and 21A,B).

As to Claim 20, Taniguchi et al. discloses, in Figs. 19, 20, 21A and 21B (Figs. 21A and 21B being variations of Figs. 19 and 20; col.14: 66-col.15: 1), a plurality of stacked packages including an upper package and a lower package, each package comprising: a board 21 having located on a first side thereof a chip installation area and a bump pad area; at least one chip 3 disposed in the chip installation area; a plurality of first bump pads 8 formed in the bump pad area electrically connected to chip 3 (by way of the wiring patterns; Figs. 19, 21A,B and col.14: 26-31), wherein the respective packages are electrically connected by connecting bump pads 8 of the upper package to bump pads 8 of the lower package (by way of bumps 7C), the chip installation area of the upper and lower packages being laterally offset from each other (Figs. 21A,B and col.15: 4-9).

6. Claims 10, 12 and 20 are rejected under 35 U.S.C. 102(b) as being anticipated by Behlen et al.

As to Claim 10, Behlen et al. discloses, in Figs. 3-6, a plurality of stacked packages including an upper package and a lower package, each package comprising: a board 312 having located on a first side 322 thereof a chip installation area 312a and a bump pad area 312b; at least one chip 310 disposed in chip installation area 312a; a plurality of redistribution patterns T1, T2, T3, T4 formed on the board and electrically connected to the chip 310 (Fig. 6; col.5: 62-col.6: 21); a plurality of first bump pads 326 formed in bump pad area 312b which are electrically connected to redistribution patterns T1, T2, T3, T4 (Fig. 6; col.5: 62-col.6: 21), wherein the respective packages are electrically connected by connecting bump pads 326 of the upper package to bump pads 326 of the lower package (Fig. 6), the chip installation area 312a of the upper and lower packages not being in vertical alignment with each other (Fig. 4).

As to Claim 12, Behlen et al. further discloses the chip installation area 312a is positioned on about ½ of the first side 322 of the board 312 (Figs. 3 and 5).

As to Claim 20, Behlen et al. discloses, in Figs. 3-6, a plurality of stacked packages including an upper package and a lower package, each package comprising: a board 312 having located on one side 322 thereof a chip installation area 312a and a bump pad area 312b; at least one chip 310 disposed in the chip installation area 312a; a plurality of first bump pads 326 formed in the bump pad area 312b electrically connected to chip 310 (col.5: 62-col.6: 21); wherein the respective packages are electrically connected by connecting bump pads 326 of the upper package to bump pads 326 of the lower package (Fig. 6), the chip installation area 312a of the upper and lower packages being laterally offset from each other (Fig. 4).

7. Claims 10, 11 and 20 are rejected under 35 U.S.C. 102(b) as being anticipated by Asada.

As to Claim 10, Asada discloses, in Figs. 8A and 8B, a plurality of stacked packages including an upper package and a lower package, each package comprising: a board (601, 602, 603, 604) having located on a first side thereof a chip installation area (at center portion of board) and a bump pad area (at peripheral portion of board); at least one chip (131, 132, 133, 134) disposed in the chip installation area; a plurality of redistribution patterns (611a-j, 612a-j, 613a-j, 614a-j) formed on the board and electrically connected to the chip (131, 132, 133, 134); a plurality of first bump pads (621a-j, 622a-j, 623a-j, 624a-j) formed in the bump pad area which are electrically connected to redistribution patterns (611a-j, 612a-j, 613a-j, 614a-j), wherein the respective packages are electrically connected by connecting bump pads of the upper package (say, bump pads 624a-j of package board 604, for example) to bump pads of the lower package (i.e., pads 623a-j of package board 603), the chip installation area of the upper and lower packages not being in vertical alignment with each other (i.e., they overlap in a laterally offset configuration).

As to Claim 11, Asada further discloses an encapsulation member 621-624 (Figs. 8A and 8B, but best seen as member 621 in Fig. 8A) surrounding the chip (note the fillet portion of the encapsulant on the side edges of the chip) inherently protecting the chip from the external environment.

As to Claim 20, Asada discloses, in Figs. 8A and 8B, a plurality of stacked packages including an upper package and a lower package, each package comprising: a board (601, 602, 603, 604) having located on a first side thereof a chip installation area (at center portion of board) and a bump pad area (at peripheral portion of board);

at least one chip (131, 132, 133, 134) disposed in the chip installation area; a plurality of first bump pads (621a-j, 622a-j, 623a-j, 624a-j) formed in the bump pad area electrically connected to the chip (131, 132, 133, 134) (by way of conductor patterns 611a-j, 612a-j, 613a-j, 614a-j), wherein the respective packages are electrically connected by connecting bump pads of the upper package (say, bump pads 624a-j of package board 604, for example) to bump pads of the lower package (i.e., pads 623a-j of package board 603), the chip installation area of the upper and lower packages being laterally offset from each other.

8. Claims 10, 14 and 20 are rejected under 35 U.S.C. 102(e) as being anticipated by Nishimura et al.

As to Claim 10, Nishimura et al. discloses, in Figs. 14 and 15, a plurality of stacked packages including an upper package and a lower package, each package comprising: a board (1a, 1b) having located on a first side thereof a chip installation area and a bump pad area (col.11: 47-51); at least one chip disposed in the chip installation area (3c in the upper package and 3b in the lower package); a plurality of redistribution patterns (i.e., the traces that connect the chip bumps 8 to the package bumps 7) formed on the board and electrically connected to the chip (3c, 3b); a plurality of first bump pads (5a, 5b) formed in the bump pad area which are electrically connected to the redistribution patterns (Figs. 14 and 15; col.11: 47-51), wherein the respective packages are electrically connected by connecting the bump pads 5a of the upper package to bump pads 5b of the lower package, the chip installation area of the upper and lower packages not being in vertical alignment with each other (e.g., compare the chip installation area for chip 3c in the upper package with the chip installation area for chip 3b in the lower package; they overlap in a laterally offset configuration).

As to Claim 14, Nishimura et al. further discloses, in Fig. 15, at least one electronic device 3d is disposed on board 1a of the upper package, and is electrically connected to the first bump pads 5a--pads 5a shown in both Figs. 14 and 15 but labeled only in Fig. 14--of the upper package (col.12: 36-39).

As to Claim 20, Nishimura et al. discloses, in Figs. 14 and 15, a plurality of stacked packages including an upper package and a lower package, each package comprising: a board (1a, 1b) having located on a first side thereof a chip installation area and a bump pad area (col.11: 47-51); at least one chip disposed in the chip installation area (3c and 3d in the upper package and 3b in the lower package); a plurality of first bump pads (5a, 5b) formed in the bump pad area electrically connected to the chip (3b, 3c, 3d) (Figs. 14 and 15; col.11: 47-51), wherein the respective packages are electrically connected by connecting bump pads 5a of the upper package 1a to bump pads 5b of the lower package 1b (Figs. 14 and 15), the chip installation area of the upper and lower packages being laterally offset from each other (Fig. 15).

Allowable Subject Matter

9. Claims 2, 3, 7, 9, 17 and 19 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

10. As allowable subject matter has been indicated, applicant's reply must either comply with all formal requirements or specifically traverse each requirement not complied with. See 37 CFR 1.111(b) and MPEP § 707.07(a).

Conclusion

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to John B. Vigushin whose telephone number is 571-272-1936. The examiner can normally be reached on 8:30AM-5:00PM Mo-Fri.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamand Cuneo can be reached on 571-272-1957. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

John B. Vigushin

John B. Vigushin
Primary Examiner
Art Unit 2841

jbv
October 16, 2005